IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 5, line 9 is amended as follows:

In accordance with the present invention, shown in Figure 5 is an interface 44 for permitting synchronous data transfer between a first domain 46 clocked at one frequency by a secondary clock 50 and a second domain 48 clocked at another frequency by a secondary clock 52. Each of the domain clocks 50 and 52 are derived from the same high frequency source as previously described with respect to Figures 1-3. The interface 44 includes a first master and slave flip flop or the like 54 and a second master and slave flip flop or the like 56, each connected to the first domain 46. The master latches 54a and 56a of flip flops 54 and 56 are each respectively directly coupled to an input of the associated slave latch 54b and 56b of the flip flops 54 and 56. The Slave latch output for each flip flop 54, 56 is respectively feed back to a multiplexer or selector 58, 60 at the input of each master latch 54a and 56a, respectively. The Slave latch output is then multiplexed with any data from the ~~first domain 38~~ first domain 46 loaded into either master latch 54a or master latch 56a. The master latch output of master latch 54a labeled "A" and the master latch output of master latch 54b labeled "B" are multiplexed into a slave latch 62 by a multiplexer or selector 64 at the input to the slave latch 62. The multiplexer 64 and slave latch 62 gate or transfer data loaded from the first domain 46 into either the master latch 54a or the master latch 56a into the second domain 48 as will be described in more detail herein.

The paragraph beginning at page 5, line 27 is amended as follows:

The operation of the interface 44 for transferring data from the first domain 46 clocked at one frequency to the second domain 48 clocked at a slower frequency or clock speed is described by referring to the three sets of timing diagrams in Figure 6. Each set of waveforms represents a different ratio of clock frequencies between the first and second domains. Referring initially to

the 3:2 ratio waveforms or timing diagrams, the first domain 46 is clocked at 200 Mhz and the second domain 48 is clocked at 133 Mhz. The synch pulse is derived so that it begins and ends coincident with the negative edges of the faster domain clock in this case the 200 Mhz clock. As shown in Figure 6 the secondary clocks 50 and 52 for the first domain 46 (200 Mhz) and the second domain 48 (133 Mhz) are repeated in a systematic pattern with each cycle being framed by the sync pulse (vertical broken lines 66 ~~and 6A8~~ and 68). An ABsel signal is generated to alternately select either the master latch 54a of flip flop 54 or the master latch 56a of flip flop 56 for loading data from the first domain 46. For simplicity of explanation in reference to Figures 5 and 6, the output "A" of the master latch 54a corresponds to clock pulses also labeled "A" in Figure 6. When an "A" clock pulse occurs in the 200 Mhz waveform clocking the first domain 46, data will be loaded into the master latch 54a and when an "A" clock pulse occurs in the slower frequency waveform (160 Mhz, 133 Mhz or 100 Mhz) the data loaded in the master latch 54a will be transferred or gated to the second domain 48 through the slave latch 62. Similarly, the output "B" of the master latch 56a for flip flop 56 corresponds to clock pulses also labeled "B" in Figure 6. When a "B" pulse occurs in the 200 Mhz waveform clocking the first domain 46, data will be loaded into the master latch 56a and when a "B" pulse occurs in the slower frequency waveform clocking the second domain, the data loaded in the master latch 56a will be transferred or gated to the second domain 48 from slave latch 62. . The ABsel select signal is generated to select the other of master latches 54a or 56a in response to or by a positive edge of an "A" or "B" pulse for loading data into one of the master latches 54a or 56a. For example, when a "B" pulse occurs clocking the first domain 46, data is loaded into the master latch 56a and the interface 44 is switched to the master latch 54a for receiving data when the next "A" pulse occurs. Similarly, the interface 44 will switch to the master latch 56a after an "A" pulse so that data can be loaded into the master latch 56a when the next "B" clock pulse occurs.

The paragraph beginning at page 8, line 6 is amended as follows:

Referring now to Figure 8, a timing diagram for Figure 5 is shown illustrating the transfer of data from the domain 46 to the second domain 48 in which the first domain is clocked by a slower clock (160 Mhz, 133 Mhz or 100 Mhz) compared to the second domain which is clocked by a faster clock, in this case 200 Mhz. The interface 44 will operate analogously to the previously described examples ~~were data~~ where data is being transferred from a faster clocked

domain to a slower clocked domain (Figure 6). Referring to the 3:2 set of waveforms, the first "A" pulse 86 of the 133 Mhz waveform will permit data to be loaded into the master latch 54a from the first domain 46 in Figure 5. Because of the sync pulse 88, the second domain 48 is synchronously clocked by the "A" pulse 90 of the second domain clock 52, operating at 200 Mhz in this example and the data is immediately transferred into the second domain 48 via slave latch 62. As before, the negative edge of the second domain clock pulse will cause the slave latch 62 to toggle to look at the other of the "A" or "B" output of the master latches 54a and 56a. Accordingly, the negative edge 92 of the "A" clock pulse 90 of the 200 Mhz clock will cause the slave latch 62 to switch to the "B" output of master latch 56a. To coordinate data transfer from the first and second domains 46 and 48 in this example of going from a slower clocked domain to a faster clocked domain, the next clock pulse 94 of the faster second domain clock 52 will be designated as a "HOLD" or non-operate (NOP) pulse to permit the slower clocked domain to catch up or keep up. The next "B" pulse 96 of the 133 Mhz first domain clock 50 will permit data from the first domain 46 to be loaded into the master latch 56a. The ABsel signal will be generated to toggle to master latch 54a to receive data when the first domain 46 is clocked by the next "A" pulse 98. When the second domain 48 is clocked by the next "B" pulse 100 of the second domain 200 Mhz clock 52, the data loaded into master latch 56a will be transferred via slave latch 62 to the second domain 48. As before, the negative edge 102 of the second domain "B" clock pulse 100 will generate the signal ABtransfer to cause the slave latch 62 to switch to the "A" output of master latch 54a to receive data when the next "A" pulse 104 of the second domain clock 52 occurs.